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FORM**

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Total Number of Pages in This Submission

15

Application Number

10/616,850

Filing Date

7/10/2003

First Named Inventor

DHONG

Art Unit

2819

Examiner Name

Vibol TAN

Attorney Docket Number

AUS920020711US1 (IBM 2601000)

ENCLOSURES (Check all that apply)

<input type="checkbox"/> Fee Transmittal Form	<input type="checkbox"/> Drawing(s)	<input type="checkbox"/> After Allowance Communication to TC
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Remarks

Reply to Office Action dated November 8, 2004 (14 pages).

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	CARR LLP
Signature	
Printed name	Theodore F. Shiells
Date	2/7/05
Reg. No.	31,569

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

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Typed or printed name	Bradley D. Ellis
Date	2/7/05

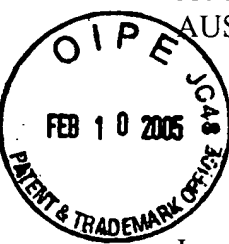
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ATTORNEY DOCKET NO.
AUS9200200711US1 (IBM 2601000)

PATENT APPLICATION
SERIAL NO. 10/616,850

DFW



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Dhong et al.

Serial Number: 10/616,850

Filed: July 10, 2003

For: INTEGRATED LOGIC AND LATCH
DESIGNS WITH CLOCK GATING AT
STATIC INPUT SIGNALS

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§
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Group Art Unit: 2819

Examiner: Tan, Vibol

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2/7/05

Bradley D. Ellis
Bradley D. Ellis

RESPONSE

Dear Sir:

In response to the Office Action dated November 8, 2004, ("Office Action"), Applicants
respond as follows: